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APPLICATION FOR UNITED STATES LETTERS PATENT

APPLICANT:	**CRAWFORD, E. J.**
FOR:	**FIB/RIE METHOD FOR IN-LINE CIRCUIT MODIFICATION OF MICROELECTRONIC CHIPS CONTAINING ORGANIC DIELECTRIC**
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FIB/RIE METHOD FOR IN-LINE CIRCUIT MODIFICATION OF MICROELECTRONIC CHIPS CONTAINING ORGANIC DIELECTRIC

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to repair or circuit modification of microelectronic chips particularly during manufacture. More specifically, chips having conductors, typically copper or aluminum, embedded in organic dielectric layers can be modified after the conductors have been formed. This organic dielectric layer is also variously described in the art by terminology such as low-k dielectric, spin-on glass, or spin-on dielectric.

Description of the Related Art

The Focused Ion Beam (FIB) tool is well known in the art for ion milling and has been used for chip analysis, modification, and repair. A typical conventional system utilizes bromine gas and a focused ion beam to selectively mill aluminum lines in a silicon oxide dielectric, a procedure that slices through the conductor to create an electrical open circuit. The complementary procedure of adding conductive material to create shorts or to connect two conductors is done by ion-assisted deposition of a metal such as tungsten from a gaseous metal precursor onto the area to be connected. This conventional method of creating electrical disconnections is not applicable to organic dielectric/ metallization

schemes because no gas is commercially available that ensures the complete removal of residual metal, such as copper, in the milled area. More important, ion milling utilizes charged ions that impregnate the organic dielectric to defeat electrical isolation.

Conventional methods using FIB milling concern aluminum lines in silicon oxide and does not work for tight pitch copper lines in low-k dielectric materials. Thus, until now no effective method exists to allow circuit modification of chips with organic dielectric layers. The disclosed technique overcomes the above mentioned problems of charged ions and residual metal by using a combination of selective dielectric removal and FIB milling.

SUMMARY OF THE INVENTION

In view of the foregoing and other problems of the conventional methods, it is, therefore, an object of the present invention to provide a method for repairing metal lines in low-k organic dielectrics.

It is another object of the invention to allow real-time circuit modifications on-chip on such chips when a circuit design change needs to be evaluated or a mask error needs to be corrected.

It is another object of the invention to allow conductor lines in low-k organic dielectrics to be selectively disconnected or selectively connected.

It is another object of the invention to improve yields on such chips, especially on large area chips where chip interconnect problems can be a major yield detractor.

It is another object of the invention to allow repairs on chips having organic dielectric/metal combinations, especially when conductor lines are closely spaced.

In a first exemplary aspect, a method for making an organic dielectric/copper modification involves: depositing an inorganic dielectric material such as nitride to form a surface protective layer; making an opening above the selected work area through this protective layer either by ion milling or by a standard mask/resist process; removing organic dielectric material adjacent to the targeted copper line by an oxygen Reactive Ion Etching (RIE) process; and, modifying the exposed conductor by either cutting the copper line by FIB milling (typically with a passivating gas such as xenon diflouride) or by depositing more conductive material to form a connection to another conductor. Repairs would normally be followed by routine deposition of an insulating layer such as silicon oxide to fill in the void of the removed organic dielectric and then a planarization process to equalize surface contours. Repairs of underlying conductors can be done by executing the basic process for each successive underlying dielectric layer.

With the invention, the problem in the prior art is overcome in which ion milling creates charged ions that impregnate the organic dielectric to defeat electrical isolation. The invention also overcomes the problem in the prior art of electrically conductive metal residue from ion milling being deposited on the sidewalls around the milled area, defeating electrical isolation.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figures 1(a) through 1(d) illustrate the basic technique for a single organic dielectric layer and one conductor;

Figure 2 is a flow chart for a preferred method 200 of the invention with a single layer, as illustrated by Figures 1(a) through 1(d);

Figures 3(a) through 3(c) illustrate the technique as extended for multiple layers; and

Figure 4 is a flow chart for a preferred method 400 as extended to multiple layers, as illustrated by Figures 3(a) through 3(c).

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

Referring now to the drawings, generally, the invention utilizes a combination of FIB (Focused Ion Beam) and RIE (Reactive Ion Etching) techniques to repair conductor lines on chips that use organic dielectric. Figures 1(a) through 1(d), as summarized by the

flowchart on Figure 2, illustrate the steps of one exemplary embodiment of the invention for a single layer.

Figure 1(a) shows a cross section of a portion of a chip 1 having organic layer 2 in which is embedded a conductor 4, typically a metal such as copper or aluminum. In this example, conductor 4 is considered to be a copper line. In general, the organic dielectric layer 2 will be isolated from underlying layers (not shown) by a protective layer 6, typically a nitride barrier layer. Such organic dielectric layers are known in the art under various terms, including low K dielectric, low conductivity dielectric, and spin-on glasses (SOG). Since it is applied as a thin film liquid, the primary advantage of spin-on dielectrics is the simplicity of applying a layer to a wafer. Although copper line 4 appears in the cross section in Figure 1(a) as lying on top of organic dielectric 2, the line is typically embedded in the layer so that the organic dielectric material is in contact with both sides as well as the bottom of copper line 4.

Wafers with chips to be repaired are removed from the manufacturing flow. Of course, this initial step is not to be interpreted as a limitation of the invention, since the disclosed process can be carried out at any stage of manufacture, including a completed chip.

As shown in the flowchart in Figure 2, a first step (S201) of the inventive method 200 is the application of a protective barrier layer 8 of inorganic material on the surface of the chip. Typically, this step includes the deposition of nitride, but other inorganic materials such as an oxide could be used.

Next, a window 10 in barrier layer 8 is opened (S203) over the area to be modified. This window could be created by FIB-ion-milling through the nitride barrier 8), shown in Figure 1(a) as beams 12 impinging on the surface. Alternatively, the window could be formed by a standard process in which an organic resist is deposited in a masked pattern so that the nitride barrier is left exposed for a standard etching process such as RIE. Both techniques for opening a window are well known in the art. Other techniques are possible, but the window cannot be created with techniques that would damage the underlying copper line.

The wafer is then etched (S205) using a RIE process selective to the organic dielectric such that the dielectric is removed between metal features in the exposed area only. Typical RIE gas mixtures for removing organic dielectrics contain varying amounts of oxygen. This etching is shown in Figure 1(b) as arrows 14, and the etching process results in a removal of the organic dielectric adjacent to targeted line 4, as shown by void area 16 and would typically remove the dielectric on each side of and partially below the targeted line to isolate the line from the surrounding dielectric. The amount of material removed below the line is not critical for a single conductor modification. This RIE etching is well known in the art and details are routinely determined experimentally for specific dielectrics and layer depths.

The modification to line 4 could be either that of connecting to another line (not shown) or cutting through line 4 to disconnect. The connection process typically includes FIB-assisted deposition of tungsten or molybdenum and is well known in the art.

Illustrated in this discussion of a preferred embodiment is the process of cutting through line 4 to create a disconnect.

To make the disconnect of line 4, the wafer is returned to the FIB for ion milling (S207) through the line. Figure 1(c) shows milled-out section 20 having been achieved by FIB beams 18 so that line 4 is now disconnected. For closely-spaced copper conductors, gas assisted etch using xenon difluoride may be employed to ensure disconnection. Shown in Figure 1(d), an insulating layer 22, typically SiO_2, is then deposited (S209) to fill the empty spaces. Finally, planarization (S211) is typically done to level off the surface and avoid effecting higher level processing, using any of well known alternative techniques.

Figures 3(a)-3(c), as summarized by the flowchart in Figure 4, illustrate an extension of the basic technique for multiple layers. Figure 3(a) shows a planar view of a surface conductor 32. An underlying conductor 30 is the target to be modified. The overlying conductor 32 is shown as an Mx copper wide line and the underlying conductor 30 is shown as an Mx-1 copper line but other scenarios would be obvious from the following discussion. To reach the underlying conductor 30, a first window 34 is opened in the upper conductor 32 and then a second window 36 is opened to allow removal of the dielectric around lower conductor 30. Any number of layers can be reached using a repeated process of the basic technique discussed above with variations to accommodate specific aspects of each circuit.

Figure 3(b) shows upper conductor 32 in upper organic dielectric layer 38 and lower conductor 30 in lower organic dielectric layer 40. Isolation layer 42 separates the upper and lower layers, and lower layer 40 has a bottom isolation layer 44 separating the lower layer 40 from another (not shown) lower layer.

Figure 4 shows a method 400 in which a protective layer 46 is applied (S401), followed by window opening of protective layer 46 (S403) to expose a work area of the upper conductor 32. Note that in this example the upper conductor is actually larger than the target work area and so there is no way to remove organic dielectric around the sides of the upper conductor. So in this case, unlike the single-conductor technique discussed above, the upper conductor 32 is milled (S405) before evacuating the associated dielectric 38 (S407). In this example any sidewall deposition of copper is acceptable since no isolation is needed due to the isolation nitride barrier 42 and because the wide line upper conductor 32 completely covers the organic layer in the work area.

This milling leaves hole 48 in upper conductor 32. The removal (S407) of organic dielectric underlying the upper conductor 32 would typically be by FIB milling followed by oxygen RIE deep enough to reach nitride barrier layer 42, leaving void 50 under upper conductor 32. Separation nitride layer 42 is then etched away (S409) with RIE or FIB milling to create the lower window 36 (see Figure 3(a)).

Removal (S411) of the organic dielectric 40 is required prior to milling of the conductor 30 to create void 52 around the conductor (see Figure 3(c)). Lower conductor 30 can then be milled to create a disconnect 54 (S413) of the lower conductor. The voids

50,52 could then be filled in as appropriate with an insulator as done in the basic technique (S415).

The above disclosed technique allows conductor lines in low-k dielectrics to be selectively disconnected or selectively connected and solves the problem in the prior art in which ion milling creates charged ions that impregnate the organic dielectric to defeat electrical isolation. The inventive technique improves yields on chips having organic dielectric layers, especially on large area chips where chip interconnect defeats can be a major detractor and is especially useful when conductor lines are closely spaced.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.